

**UNITED STATES DEPARTMENT OF COMMERCE****Patent and Trademark Offic**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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09/031,326 02/26/98 KARNIEWICZ

J 303.376US1

021186
SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH
P.O. BOX 2938
MINNEAPOLIS MN 55402

TMX2/0131

EXAMINER

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ART UNIT	PAPER NUMBER
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2123

DATE MAILED:

01/31/01

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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

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Office Action Summary

Application No. 09/031,326	Applicant(s) Joseph J. Karniewicz
Examiner Thai Phan	Group Art Unit 2123



Responsive to communication(s) filed on Aug. 04, 2000

This action is FINAL.

Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1035 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claim

Claim(s) 1-25 is/are pending in the application.
Of the above, claim(s) _____ is/are withdrawn from consideration.
 Claim(s) _____ is/are allowed.
 Claim(s) 1-25 is/are rejected.
 Claim(s) _____ is/are objected to.
 Claims _____ are subject to restriction or election requirement.

Application Papers

See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.
 The drawing(s) filed on _____ is/are objected to by the Examiner.
 The proposed drawing correction, filed on _____ is approved disapproved.
 The specification is objected to by the Examiner.
 The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).
 All Some* None of the CERTIFIED copies of the priority documents have been
received.
 received in Application No. (Series Code/Serial Number) _____
 received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

Notice of References Cited, PTO-892
 Information Disclosure Statement(s), PTO-1449, Paper No(s). 08
 Interview Summary, PTO-413
 Notice of Draftsperson's Patent Drawing Review, PTO-948
 Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

This official action is in response to applicant's amendment filed on Aug. 04, 2000.

Claims 1-25 are pending in this official action.

1. Acknowledgment has been made for the submission of copending application serial data.
2. Acknowledgment has been made for the drawings correction.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

4. Claims 1-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Heile et al., patent no. 5,983,277.

As per claims 1 and 9, Heile anticipates method and system of workstations, databases for shared memory, etc. for populating parameters of cells (Abstract, Figs. 3-12) for use in circuit

design environment identical to the claimed invention. According to Heile, the design apparatus includes global files of global variables and design database (col. 2, line 65 to col. 3, line 46, col. 9, lines 12-23), a plurality of local files, each relating a plurality of local variables to the global variables (col. 6, lines 21-36, col. 8, lines 41-67, col. 9, lines 1-12), and a plurality of cells, each cell corresponding to a local file and having a set of parameters derived by relating the local variables to the global variables in the global source files such that the changes of global variables in the global files reflect or may cause changes in the cells (Figs. 3-12, col. 9, lines 40-60, col. 10, lines 7-24, lines 44-59, cols. 11, 12, 14-18, for example).

As per claims 2-3 and 10-11, Heile disclosed local files include inherent file from source files, instance files, etc. (Figs. 3-12).

As per claim 4, Heile disclosed master files acting as initial version of a corresponding local file for design, modification, increment compilation, etc.

As per claim 5, Heile disclosed file or clean sheet file for containing design rules for a plurality of cells for coordinated design as claimed.

As per claim 6, Heile disclosed file extraction and related variable extraction for design and update design.

As per claims 7-8, Heile anticipated the design display in local users.

As per claim 12, Heile disclosed file update including update global file for coordinate process.

As per claim 13, Heile anticipated local display in local user workstation in design process.

As per claim 14, Heile disclosed computer program in concurrent with design program for circuit design process as claimed.

As per claim 15, anticipates method and system of workstations, databases, shared memory, etc. for populating parameters of cells (Abstract, Figs. 3-12) for use in circuit design environment identical to the claimed invention. According to Heile, the design apparatus includes local user work stations, central workstations, global files of global variables and design database, system memory for sharing between users (col. 2, line 65 to col. 3, line 46, col. 9, lines 12-23), a plurality of local files, each relating a plurality of local variables to the global variables (col. 6, lines 21-36, col. 8, lines 41-67, col. 9, lines 1-24), and a plurality of cells, each cell corresponding to a local file and having a set of parameters derived by relating the local variables to the global variables in the global source files such that the changes of global variables in the global files reflect or may cause changes in the cells (Figs. 3-12, col. 9, lines 40-60, col. 10, lines 7-24, lines 44-59, cols. 11, 12, 14-18, for example) or updating variables in local file by reading from the global file value of global variables to which the local variables of the local file correspond (col. 10, line 35 to col. 12, line 50, col. 13, lines 24-43, lines 51-64, for example) as claimed.

Similarly, claims 16-21 are also rejected due to its similarities to claims 2-8 and claims 11-14.

Claim Rejections - 35 USC § 102

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

5. Claims 22-25 are rejected under 35 U.S.C. 102(e) as being clearly anticipated Van Huben et al., patent no. 6,035,297.

As per claim 22, Van Huben disclosed method and system for design of integrated circuit, circuit verification using a database structure for storing and accessing data (Abstract, cols. 2-7, Fig. 1) identical to the claimed invention. According to Van Huben, the design system includes a global file of global variables (col. 5, line 50 to col. 6, line 35), a plurality of local files relating to local variables to the global variables (Figs. 10-13, 16-20, col. 6, line 40 to col. 7, line 62, col. 12, lines 42-53, cols. 30-32, for instance), and local files in the templates containing a plurality of cells (cols. 30-32, col. 34, line 35 to col. 35, line 38, col. 38-43, for example).

Van Huben also disclosed the design process and verification could be implemented in computer programming languages such as C, Java, etc., this would include computer programming language such as SKILL as claimed. SKILL programming language in conjunction with Design Framework II as claimed is known in the art, and being used by applicant in the design process. It would inherently be for practitioner in the art to use such available tools to implement the circuit design process, or other design processes as taught by Van Huben to provide an efficient method to implement the verification process. Van Huben also disclosed

design rules files in templates of various platforms for forming a set of global variables and setting/updating values for such variables for the design process and verification by request by users as claimed.

As per claims 23-24, VanHuben anticipated inherent file, and instance file in the design database.

As per claim 25, Van Huben anticipated design framework for use in the chip design process. Such framework could be known CADENCE Design system as claimed.

Response to Arguments

6. Applicant's arguments filed Aug. 04, 2000 have been fully considered but they are not persuasive.

In response to applicant's argument the amended features as in amended claims 1 and 9 (page 3, last paragraph to page 4, paragraph 2), the examiner responds such amended features are well anticipated in the art. In fact, Heile anticipated method and system for populating parameters of cells in a design environment which include a global work space and a plurality of user workspaces (Abstract, Figs. 3-12, col.3, lines 1-29, col. 6, lines 21-36, col. 8, lines 41-67, cols. 9-16).

In response to applicant's argument the amended feature of "reading, from the global file, values for the global variables to which the local variables of the local file correspond" as amended in claim 15 (page 4, paragraph 2), the examiner responds such feature is well anticipated in the art. Heile anticipated design system includes the features as claimed. The

design system includes database management system which updates variables in local file by reading from the global file value of global variables to which the local variables of the local file correspond (col. 10, line 35 to col. 12, line 50, col. 13, lines 24-43, lines 51-64, for example) for use in coordinate design and shared memory system.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thai Phan whose telephone number is (703) 305-3812.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703)305-3900.

Any response to this final action should be mailed to:

Box AF

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 308-9051, (for formal communications; please mark "EXPEDITED PROCEDURE"),

Or:

(703) 308-1396 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA., Sixth Floor (Receptionist).

January 29, 2001



KEVIN J. TESKA
SUPPLY/ADVISORY
PATENT